IN THE CLAIMS

1. (Original) A digital camera comprising:

a control subsystem comprising a microprocessor;

an imaging subsystem in communication with the controlled subsystem; and

a power management subsystem in communication with the control subsystem, the power management subsystem comprising:

power selection-isolation circuitry for isolating at least two power sources;

battery charging circuitry in communication with the power selection-isolation circuitry; and

power arbitration circuitry in communication with the power selection-isolation circuitry and the battery charging circuitry.

2. (Original) The digital camera of claim 1 further comprising a user interface subsystem for providing a camera status and initiating a camera function.

3. (Original) The digital camera of claim 2 wherein the power arbitration circuitry comprises:

a camera wakeup generation module in communication with the user interface subsystem; and

a failsafe reset module in communication with the wakeup generation module and the microprocessor.

4. (Original) The digital camera of claim 3 wherein the user interface subsystem comprises:

a user accessible actuator for implementing a camera function;

an inverter having an input in communication with the user accessible actuator and an output in communication with the wakeup generation module;

an active pull-up latch in communication with the inverter input and the inverter output;

a first active pull-up in communication with the inverter input adapted to receive a first control signal; and

a second active pull-up in communication with the inverter input adapted to receive a second control signal.

5. (Original) The digital camera of claim 4 wherein the user accessible actuator comprises a switch.

6. (Original) The digital camera of claim 4 wherein the user accessible actuator comprises a button.

7. (Original) The digital camera of claim 4 wherein the first control signal comprises a strobed signal.

8. (Original) The digital camera of claim 4 wherein the second control signal comprises a logic signal active at a power off state.

9. (Original) The digital camera of claim 1 wherein the battery charging circuitry comprises:

a first transistor having a first active area;

a second transistor having a second active area, the second transistor connected to the first transistor in a differential configuration; and

at least one supplemental transistor having a supplemental active area, the supplemental transistor connected in series with a supplemental switch, the supplemental transistor and supplemental switch further connected in parallel with the second transistor.

10. (Original) The digital camera of claim 9 wherein the second active area is about ten times the first active area.

11. (Original) The digital camera of claim 9 wherein the supplemental switch has a state established by a firmware instruction.

12. (Original) The digital camera of claim 1 wherein the power selection-isolation circuitry comprises a power arbitration circuit comprising:

a battery power bus;

an external power bus;

a first transistor adapted to receive a battery enabling signal, the first transistor having a first shunt diode, the first shunt diode having a first shunt anode and a first shunt cathode, the first shunt anode in communication with the battery power bus; and

a second transistor adapted to receive a bus enable signal, the second transistor having a second shunt diode, the second shunt diode having a second shunt anode and a second shunt cathode, the second shunt anode in communication with the external power bus and the second shunt cathode in communication with the first shunt cathode.

13. (Original) The digital camera of claim 12 wherein the first shunt diode comprises a parasitic component of the first transistor.

14. (Original) The digital camera of claim 12 wherein the second shunt diode comprises a parasitic component of the second transistor.

15. (Original) The digital camera of claim 1 wherein the power selection-isolation circuitry comprises:

a battery power bus;

an external power bus;

a first transistor adapted for receiving a shutdown signal having a first shunt diode, the first shunt diode having a first shunt anode and a first shunt cathode, the first shunt cathode in communication with the external power bus;

a second transistor adapted for receiving the shutdown signal having a second shunt diode, the second shunt diode having a second shunt anode and a second shunt cathode, the second shunt anode in communication with the first shunt anode; and

a third transistor adapted for receiving a control signal having a third shunt diode, the third shunt diode having a third shunt anode in communication with the battery power bus, and a third shunt cathode in communication with the second shunt cathode.

16. (Original) The digital camera of claim 15 wherein the first shunt diode comprises a parasitic component of the first transistor.

17. (Original) The digital camera of claim 15 wherein the second shunt diode comprises a parasitic component of the second transistor.

18. (Original) The digital camera of claim 15 wherein the third shunt diode comprises a parasitic component of the third transistor.

19-37 (Cancelled)

38. (Original) A digital camera comprising:

a means for controlling operation;

a means for acquiring an image;

a means for managing power in communication with the acquiring means, the power-management means comprising:

a means for controlling power

a means for charging a battery in communication with the power-control means;

a means for arbitrating power in communication with the power-control means and the battery-charging means.